WHAT IS CLAIMED IS:

1. A method of buffering an RF signal comprising:

receiving an input signal, wherein the input signal alternates between a first polarity and a second polarity;

generating a first current, wherein the first current is proportional to the input signal when the input signal has the first polarity, and approximately equal to zero when the input signal has the second polarity;

generating a second current, wherein the second current is proportional to the input signal when the input signal has the second polarity, and approximately equal to zero when the input signal has the first polarity;

generating a third current proportional to the first current;

generating a fourth current proportional to the second current;

applying the first and fourth currents to a first terminal of an inductor; and

applying the second and third currents to a second terminal of the inductor.

2. The method of claim 1 wherein a capacitance is between the first terminal of the inductor and the second terminal of the inductor, and the inductor and capacitance form a tank circuit.

3. The method of claim 2 wherein the input signal alternates between the first polarity and the second polarity at a first frequency, the tank circuit has a resonant frequency of a second frequency, and the first frequency and second frequency are approximately equal.

4. The method of claim 2 wherein the first current and the second current are generated by NMOS devices.

5. The method of claim 4 wherein the third current and the fourth current are generated by PMOS devices.

6. The method of claim 2 wherein the first current is geometrically proportional to the input signal when the input signal has the first polarity, and the second current is geometrically proportional to the input signal when the input signal has the second polarity.

7. A circuit for buffering RF signals comprising:

a first switch coupled between a first supply node and a first output node;

a second switch coupled between the first supply node and a second output node;

a third switch coupled between the first output node and a second supply node;

a fourth switch coupled between the second node and the second supply node; and

an inductor coupled between the first output node and the second output node.

8. The circuit of claim 7 wherein the first switch, the second switch, the third switch, and the fourth switch are open or closed depending on the polarity of an input signal.

9. The circuit of claim 8 wherein when the input signal has a first polarity, the first and fourth switches are open, and second and third switches are closed.

10. The circuit of claim 9 wherein when the input signal has a second polarity, the first and fourth switches are closed, and second and third switches are open.

11. The circuit of claim 7 wherein the third switch and the fourth switch are NMOS devices.

12. The circuit of claim 11 wherein third and fourth switch are biased near their cutoff region.

13. The circuit of claim 11 wherein the first switch and the second switch are PMOS devices.

14. The circuit of claim 13 wherein the PMOS devices are configured to provide positive feedback.

15. An integrated circuit, wherein the integrated circuit comprises the circuit of claim 7.

16. A circuit for buffering RF signals comprising:

a first device coupled between a first output node and a first supply node, having a control electrode coupled to a first input node;

a second device coupled between a second output node and the first supply node, having a control electrode coupled to a second input node;

a third device coupled between a second supply node and the first output node, having a control electrode coupled to the second output node;

a fourth device coupled between the second supply node and the second output node, having a control electrode coupled to the first output node; and

an inductor coupled between the first output node and the second output node.

17. The circuit of claim 16 further comprising:

a fifth device coupled between the first device and the first output node; and

a sixth device coupled between the second device and the second output node.

18. The circuit of claim 16 wherein the first device and the second device are NMOS devices, and the third device and fourth device are PMOS devices.

19. An integrated circuit, wherein the integrated circuit comprises the circuit of claim 18.

20. A transceiver comprising the circuit of claim 18.

21. An computing device comprising:

a memory;

a central processing unit coupled to the memory; and

the transceiver of claim 20 coupled to the central processing unit.